

Confirmation No. 8831

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellant:	DYTRYCH	Examiner:	Faherty, C.
Serial No.:	10/583,052	Group Art Unit:	2183
Filed:	June 14, 2006	Docket No.:	NL031445US1 (NXPS.532PA)
Title:	MEMORY-EFFICIENT INSTRUCTION PROCESSING SCHEME		

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APPEAL BRIEF

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Commissioner For Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Customer No.  
**65913**

Dear Sir:

This Appeal Brief is submitted pursuant to 37 C.F.R. §41.37, in support of the Notice of Appeal filed November 5, 2009 and in response to the rejections of claims 1-3, 6-10 and 12-17 as set forth in the Final Office Action dated September 8, 2009.

**Please charge Deposit Account number 50-4019 (NL031445US1) \$540.00** for filing this brief in support of an appeal as set forth in 37 C.F.R. §1.17(c). If necessary, authority is given to charge/credit Deposit Account 50-0996 additional fees/overages in support of this filing.

**I. Real Party In Interest**

The real party in interest is NXP Semiconductors. The application is presently assigned of record, at reel/frame nos. 019719/0843 to NXP, B.V., headquartered in Eindhoven, the Netherlands.

**II. Related Appeals and Interferences**

While Appellant is aware of other pending applications owned by the above-identified Assignee, Appellant is unaware of any related appeals, interferences or judicial proceedings that would have a bearing on the Board's decision in the instant appeal.

**III. Status of Claims**

Claims 1-3, 6-10 and 12-17 stand rejected and are presented for appeal. Claims 4-5 and 11 are cancelled. A complete listing of the claims under appeal is provided in an Appendix to this Brief.

**III. Status of Amendments**

An amendment was filed on October 22, 2009 subsequent to the Final Office Action dated September 8, 2009, and the amendment has been entered.

**IV. Summary of Claimed Subject Matter**

As required by 37 C.F.R. § 41.37(c)(1)(v), a concise explanation of the subject matter defined in the independent claims involved in the appeal is provided herein. Appellant notes that representative subject matter is identified for these claims; however, the abundance of supporting subject matter in the application prohibits identifying all textual and diagrammatic references to each claimed recitation. Appellant thus submits that other application subject matter, which supports the claims but is not specifically identified above, may be found elsewhere in the application. Appellant further notes that this summary does not provide an exhaustive or exclusive view of the present subject matter, and Appellant refers to the appended claims and their legal equivalents for a complete statement of the invention.

Commensurate with independent claim 1, an example embodiment of the present invention is directed to a parallel processing apparatus (*see, e.g.*, FIG. 1; page 1:1-24) for

processing data based on instruction words (*see, e.g.*, FIG. 2; page 5:30-7:10) comprising at least two individual instructions (*see, e.g.*, FIG. 2, elements FUXn; page 5:30-7:10) used for controlling at least two respective functional units (*see, e.g.*, FIG. 1, elements FUN; page 5:30-7:10), said apparatus comprising: an instruction processor arranged to process a first individual instruction (*see, e.g.*, FIG. 2, elements FUXn; page 5:30-7:10) extracted from a first instruction word, and at least a second individual instruction (*see, e.g.*, FIG. 2, elements FUXn; page 5:30-7:10) extracted from at least a subsequent second instruction word, as a new single instruction word (*see, e.g.*, FIG. 2, elements FUXn; page 5:30-7:10), the instruction processor further arranged to add predetermined control information (*see, e.g.*, FIG. 2, elements CB and Iyn; page 5:30-7:10) to said single instruction word, said control information indicating an allocation of said extracted first and at least second individual instructions to said respective functional units and a sequential order of said first and at least second individual instructions at their respective functional units; and a program memory arranged to store said single instruction word.

Commensurate with independent claim 12, an example embodiment of the present invention is directed to a method of compressing instruction words each comprising at least two individual instructions (*see, e.g.*, FIG. 2, elements FUXn; page 5:30-7:10) used for controlling at least two respective functional units (*see, e.g.*, FIG. 1, elements FUN; page 5:30-7:10), said method comprising the steps of: extracting a first individual instruction from a first instruction word (*see, e.g.*, FIG. 2, elements FUXn; page 5:30-7:10); extracting at least a second individual instruction from at least one subsequent second instruction word (*see, e.g.*, FIG. 2, elements FUXn; page 5:30-7:10); generating from said first and second individual instructions a new single instruction word (*see, e.g.*, FIG. 2; page 5:30-7:10); adding predetermined control information (*see, e.g.*, FIG. 2, elements CB and Iyn; page 5:30-7:10) to said single instruction word, said control information indicating an allocation of the extracted first and at least second individual instructions to said respective functional units and a sequential order of the first and at least second individual instructions at their respective functional units; and storing said single instruction word.

## **VI. Grounds of Rejection to be Reviewed Upon Appeal**

The grounds of rejection to be reviewed on appeal are as follows:

- A. Claims 1-3, 6-7, 10 and 12-17 stand rejected under 35 U.S.C. § 103(a) over Suzuki (EP 1046983) in view of Faraboschi (U.S. Patent No. 5,930,508).
- B. Claims 8-9 stand rejected under 35 U.S.C. § 103(a) over the '983 and '508 references in view of Iwata (U.S. Patent No. 6,275,921) and further in view of Topham (U.S. Patent Pub. 2001/0047466).

## **VII. Argument**

The impropperity of the rejections is apparent for a variety of different reasons.

Perhaps the simplest of these is that the Examiner agrees with Appellant that certain aspects are not taught by (nor rendered obvious by) the prior art of record. The Examiner has not presented any correspondence to certain limitations. Accordingly, a *prima facie* case for the rejection has not been presented.

In the absence of such correspondence, the Examiner has chosen not to address the pertinent limitations. Instead of attempting to consider the claim limitations as a whole (M.P.E.P. § 2141.02) the Examiner attempts to show correspondence to a hypothetical claim that is based upon an interpretation that ignores claim limitations. There is no support for the Examiner's proposition that limitations cannot be interpreted to have "virtually no limiting effect" (Advisory Action of Nov. 3, 2009). If the limitations are present, which is undisputed, the limitations must be considered as they participate in setting forth the claim as a whole. The law does not permit the limitations to be interpreted in a manner that has "virtually no limiting effect."

As background and to assist the Boards review, Appellant presents the following overview. The general area of many of the embodiments discussed in Appellant's specification relates to very long instruction word (VLIW) processors. Appellant's specification explains that, due to interdependencies between functional units of VLIW processors, NOPs (referring to "no-operation" instructions for a processor) are often inserted

to delay processing of one or more instructions. Unfortunately, the addition of NOPs can require additional instruction memory space, which is often costly or difficult to implement. *See, e.g.*, Appellant's specification, pages 2-3.

Appellant's specification teaches certain embodiments that are directed toward compression and compaction schemes that can be useful for providing efficient solutions specially suited for low power processing units (*e.g.*, low hardware complexity and high cycle efficiency). *See, e.g.*, Appellant's specification, page 4. Specialized hardware can be used in connection with compressed instruction formatting to achieve such solutions. For instance, the following instructions sets illustrate a particular compression scheme:

“00”<FU3-I1><FU-I1><FU1-I1> //parallel format  
“01”<FU2-I1><FU2-I2><FU2-I3> // three compressed NOP||NOP||FU1 triples  
“10”<FU3-I1><FU2-I2><FU1-I2> // three compressed NOP||FU2||NOP triples  
“11”<FU3-I1><FU2-I2><FU1-I2> // compr. FU3||NOP||NOP, NOP||FU2||FU1 pairs  
-Appellant's specification, pages 6-7.

Appellant's specification explains that “FU” indicates a functional unit of the VLIW processor and “I” indicates an instruction index that designates the sequential order of the instruction at the concerned functional unit. Thus, the combination of the control information bits (*e.g.*, “00” or “01”) and the instruction index provide an elegant solution that can help realize the aforementioned aspects related to low hardware complexity and high cycle efficiency.

Turning now to the references relied upon the Examiner, the primary '983 reference provides a mechanism for assigning special bits that can be indicative of the presence or absence of a NOP. Notwithstanding, there is no dispute that the '983 reference fails to teach or suggest the use of such bits in combination with bits designating the sequential order of the instruction at the concerned functional unit.

The secondary '508 reference teaches a scheme that has important differences from the above-described scheme taught by the primary '983 reference. The scheme of the '508 reference eliminates at least a portion of syllables of NOPs. To differentiate between instructions, this scheme requires the use of a start (or stop) bit, also referred to as a delineator bit, that can be included in each syllable to indicate boundaries between

compacted instructions in memory. *See, e.g.*, the '508 reference, Col. 5:11-19. The record is undisputed that these delineator bits do not designate or indicate more than a boundary between instructions. For instance, the delineator bits contain no information that designates the order that the instructions are to be executed. For example, given two instructions separated by a delineator bit, the record does not show that the delineator bit would be different based upon whether one or the other instruction is to be executed first.

As discussed in more detail hereafter, the Examiner has presented a procedurally flawed argument that alleges that the existence of a hypothetical claim as basis to virtually ignore limitations, despite the express language of the claims. Moreover, the Examiner attempts to modify the primary '983 reference in a manner that is illogical and does not make sense in view of the Examiner's alleged reason to implement the modification.

**A. The Rejections Of Claims 1-3, 6-7, 10 And 12-17 Under 35 U.S.C. § 103(a) Are Improper For Lack Of Correspondence And Because The Proposed Modification Is Improper.**

The Examiner has chosen not to present any correspondence to limitations directed towards an indication of a sequential order at respective functional units. The Examiner provides no argument or evidence that the cited references provide an indication of a sequential order at respective functional units. Accordingly, a *prima facie* case for the rejection has not been presented.

The Examiner maintains the rejection under the guise of an interpretation of claim limitations. The Examiner, however, has instead attempted to show correspondence to a hypothetical claim that does not correspond to Appellant's claims as a whole. *See, e.g.*, Advisory Action of November 03, 2009 (the claim limitations have "virtually no limiting effect"). Thus, the Examiner has not shown correspondence to the claim limitations. It is improper to ignore limitations. The Examiner acknowledges that there is no correspondence to limitations directed toward indications of a sequential order at respective functional units. Thus, there is not a *prima facie* case of obviousness because the limitations as a whole have not been addressed. Accordingly, the record is clear that there is a lack of correspondence to the claimed invention and the rejections should be reversed.

Notwithstanding, the Examiner’s argument appears to rely upon the mistaken assumption that because a claim does not expressly recite an aspect, that aspect is necessarily absent. For instance, Appellant’s claims include limitations directed toward two different instructions. In a hypothetical embodiment, these two instructions could conceivably be sent to two different functional units. The Examiner incorrectly presumes that there are necessarily only these two instructions, and that therefore, there is no sequential order because only one instruction is present at each functional unit. The Examiner’s mistake is the assumption that there can be no other instructions. Appellant’s claims, however, are written using the transitional phrase “comprising” and thus are not so limited. A proper interpretation requires that all claim limitations be addressed including implicitly claimed aspects. Accordingly, the record is clear that there is a lack of correspondence to the claimed invention and the rejections should be reversed.

Appellant further submits that the alleged combination is neither obvious nor logical. The primary ‘983 reference uses a different scheme that has not been shown to require or to benefit from the use of the delimiters of the secondary ‘503 reference. Neither the Examiner nor the references teach or suggest that these different schemes would function together. A *prima facie* case of obviousness rejection requires a “clearly articulated” explanation for the combination. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (U.S. 2007).

The primary ‘983 reference implements a compression scheme and the secondary ‘503 reference implements a different compression scheme. The Examiner has incorrectly concluded, without sufficient articulated explanation thereof, that individual elements of one compression scheme have usefulness in the other. For instance, the compression schemes rely upon different types of coding of the data and would not be a simple one-for-one replacement or integration of elements from one into the other. The Examiner’s explanation is little more than a conclusion that does not address the problems with the combination. In particular, the Examiner’s Advisory Action states “the examiner has not relied upon the contradictory teachings in the two references.” The Examiner fails to articulate exactly what is being relied upon and how the relied upon portions function together. Moreover, the conclusion is based upon circular logic, *i.e.*, the evidence of teaching away of the references’ teachings is closely related to those aspects being relied upon. Accordingly, there is not a

*prima facie* showing of obviousness due to the absence of any clearly articulated details regarding how the combination would function. The Examiner also fails to consider evidence of nonobviousness in the form of teaching away (*see, e.g.*, M.P.E.P. § 2145). As discussed in more detail hereafter, it is not proper to selectively ignore teachings of the references for no reason other than the ignored teachings do not support the Examiner's conclusion.

The rejections are further improper because the identified delineator bits from the secondary '503 reference do not provide an indication of a sequential order for the instructions at a functional unit. The delineator bits have not been shown to have any relationship to the order of instructions at a functional unit. Moreover, the delineator bits have not been shown to indicate any sequential order. The Examiner's argument is a but-for argument that is not logically sound. The Examiner alleges that but-for the delineator bits, the instructions could not be separately decoded. This but-for argument, however, does not correlate to an indication of a sequential order. Many aspects of the instructions (*e.g.*, bit length, bit codes, data structure, stored memory locations) would also satisfy this but-for logic in so much as the system would not be able to properly decode instructions in their absence. Thus, Appellant maintains that the delineator bits do exactly what the '503 reference teaches and their name implies, they delineate between two instructions stored within memory. What they do not do, however, is indicate an order of these instructions at respective functional units. Accordingly, the record is clear that there is a lack of correspondence to the claimed invention and the rejections should be reversed.

The Examiner's dismissal of the evidence of non-obviousness in the form of teaching away and frustration of purpose is not proper. As correctly noted by the Supreme Court, inventions are nearly always composed of elements that are already known, in some form or another. *KSR* at 419. Other guidelines recognize that an examiner is necessarily afforded with knowledge of the invention, opening the door for improper hindsight reconstruction. For these and other reasons, the case law clearly prohibits combinations that would so change the underlying reference that it would cease to operate according to the primary teachings. The case law also clearly establishes that teaching away is strong evidence of non-obviousness. As such, combinations that redesign the underlying teachings in a manner that

undoes stated objectives thereof are *prima facie* invalid irrespective of whether or not they might or might not be possible. In this particular instance, the Examiner alludes to an unidentified and hypothetical compression scheme based upon “compressed instructions that do not need to meet the same criteria that instructions in the system of Suzuki must meet in order to be compressed.” No further explanation is provided for this conclusion. Thus, the record does not support that the references teach or suggest any such a combination.

For instance, the addition of delimiter encoding bits into the system of the primary ‘983 reference would not provide the stated benefits and would frustrate the purpose of the ‘983 reference. The secondary ‘503 reference teaches that the delineator bits are necessary to delineate between instructions stored within memory. The primary ‘983 reference has not been shown to suffer from problems related to storage of instruction words across address boundaries. Fig. 3 of the ‘983 reference shows that the system is designed so that the stored instructions 15 can be easily transferred to respective left and right containers 2,3. This is accomplished through a specific coding and compression scheme discussed in detail in the ‘983 reference. In contrast, the secondary ‘503 reference uses a very different scheme that is not designed in a manner consistent with the ‘983 reference’s simple transfer to respective left and right containers. As such, the secondary ‘503 reference is subject to problems that do not exist in the context of the ‘983 reference. The skilled artisan would not seek to modify the primary ‘983 reference to fix problems that do not exist. Thus, the proposed modification serves no identifiable purpose and appears only to increase the size of the instruction in direct contradiction to a stated purpose of the ‘983 reference. Moreover, a hypothetical and significant redesign of the ‘983 reference would be *prima facie* invalid as the resulting system would cease to function consistent with the functionality taught by the ‘983 reference.

For each of the aforementioned reasons, the rejections are improper and should be reversed.

**B. The Rejections Of Claims 8-9 Under 35 U.S.C. § 103(a) Are Improper For Lack Of Correspondence And Because The Proposed Modification Is Improper.**

The rejections of claim 8-9 rely upon the same underlying combination of references as discussed above in section A. The addition of the ‘921 reference and the ‘466 reference do not overcome (nor are they alleged to overcome) these deficiencies. Accordingly, the rejections are improper and should be reversed for each of the reasons presented above in section A, which are not repeated here for the sake of brevity.

Moreover, the rejections are improper for failing to show correspondence to the claim limitations as a whole and for improperly relying upon vague generalities and unknown hypothetical embodiments that are not clearly articulated. The references do not provide guidance on how to implement the Examiner’s proposed modification within the context of the primary ‘983 reference. The hypothetical modification appears to be conclusion that given a vague notion of a concept it would have been obvious to try the concept in the specific context of the primary ‘983 reference as modified by the secondary ‘503 reference. For instance, the Examiner’s alleged modification is to use aspects from the ‘983 reference for the purpose of marking “those specific types of instructions in order to analyze them for potential extraction.” *Final Office Action*, Sept. 9, 2009, pages 5-6. The primary ‘983 reference is taught to function without any such a modification and the Examiner’s vague hypothetical modification has not been articulated with enough particularity to be understood. Appellant has therefore not been afforded an opportunity to assess the proposed modification because it is no more than a vague conclusion that modifications would be obvious. Such arguments find little, if any, support in the teachings of the references as a whole and strongly suggest that the Examiner is using improper hindsight reconstruction based upon teachings gleaned only from Appellant’s specification.

For each of the aforementioned reasons, the rejections are improper and should be reversed.

**VIII. Conclusion**

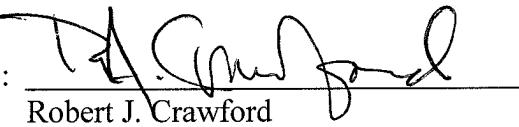
In view of the above, Appellant submits that the rejections of claims 1-3, 6-10 and 12-17 are improper and therefore requests reversal of the rejections as applied to the appealed claims and allowance of the entire application.

Authority to charge the undersigned's deposit account was provided on the first page of this brief.

*Please direct all correspondence to:*

Corporate Patent Counsel  
NXP Intellectual Property & Standards  
1109 McKay Drive; Mail Stop SJ41  
San Jose, CA 95131

CUSTOMER NO. 65913

By:   
Robert J. Crawford  
Reg. No.: 32,122  
Shane O. Sondreal  
Reg. No.: 60,145  
651-686-6633  
(NXPS.532PA)

**APPENDIX OF CLAIMS INVOLVED IN THE APPEAL**  
(S/N 10/583,052)

1. A parallel processing apparatus for processing data based on instruction words comprising at least two individual instructions used for controlling at least two respective functional units, said apparatus comprising:
  - an instruction processor arranged to process a first individual instruction extracted from a first instruction word, and at least a second individual instruction extracted from at least a subsequent second instruction word, as a new single instruction word, the instruction processor further arranged to add predetermined control information to said single instruction word, said control information indicating an allocation of said extracted first and at least second individual instructions to said respective functional units and a sequential order of said first and at least second individual instructions at their respective functional units; and
  - a program memory arranged to store said single instruction word.
2. An apparatus according to claim 1, wherein said instruction processor is arranged to extract said first and at least second individual instructions if said first and at least second instruction words each comprise one of predetermined instruction patterns with at least one delay instruction, and to compress said first and at least second instruction words into said single instruction word.
3. An apparatus according to claim 2, wherein said delay instruction is a null operation.
6. An apparatus according to claim 1, wherein said control information further includes at least one bit added as at least one respective most significant bit to said single instruction word.
7. An apparatus according to claim 1, wherein said instruction processor arranged to check said control information in an instruction word read from the program memory to re-establish said first and at least second instruction words based on said control information,

and to supply said re-established first and at least second instruction words to an instruction decoder.

8. An apparatus according to claim 1, wherein said instruction processor is arranged to mark all instruction words associated with delay slots and branch targets, and to decide on extraction of said first and at least second individual instructions based on the markings.

9. An apparatus according to claim 8, wherein said instruction processor is arranged to adjust at least one program memory address based on a decided extraction.

10. An apparatus according to claim 1, wherein said parallel processing apparatus is a VLIW processor.

12. A method of compressing instruction words each comprising at least two individual instructions used for controlling at least two respective functional units, said method comprising the steps of:

extracting a first individual instruction from a first instruction word;

extracting at least a second individual instruction from at least one subsequent second instruction word;

generating from said first and second individual instructions a new single instruction word;

adding predetermined control information to said single instruction word, said control information indicating an allocation of the extracted first and at least second individual instructions to said respective functional units and a sequential order of the first and at least second individual instructions at their respective functional units; and

storing said single instruction word.

13. A computer readable storage medium storing executable instructions which, when loaded into a computer, cause the computer to perform the steps of a compression method according to claim 12.

14. An apparatus according to claim 1, wherein said new single instruction word further includes a third individual instruction extracted from a subsequent third instruction word.
15. An apparatus according to claim 14, wherein the predetermined control information of the new single instruction word further indicates at least one of a functional unit allocation of the extracted third individual instruction and a sequential order of the third individual instruction at an associated functional unit.
16. A method according to claim 12, wherein the added control information further includes at least one bit added as at least one respective most significant bit to said single instruction word.
17. A method according to claim 12, further comprising:
  - reading the stored single instruction word;
  - checking said control information in the read single instruction word;
  - re-establishing said first and at least second instruction words based on said control information; and
  - decoding said re-established first and at least second instruction words.

## **APPENDIX OF EVIDENCE**

Appellant is unaware of any evidence submitted in this application pursuant to 37 C.F.R. §§ 1.130, 1.131, and 1.132.

## **APPENDIX OF RELATED PROCEEDINGS**

As stated in Section II above, Appellant is unaware of any related appeals, interferences or judicial proceedings.